Semiconductor Protection Mechanisms: an Industry Point of View

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By:

Walter D. Scott, Jr.

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Preface

"Semiconductor Industry Remains Unbounded. Global demand for semiconductors continues to rocket ahead."

These headlines are from the Henderson Electronic Market Forecast, dated April 1995. The semiconductor industry is on a roll. This report outlines the protection mechanisms available to the semiconductor industry and addresses the question, is mask works registration a viable means of protection for semiconductors, 11 years after the Semiconductor Chip Protection Act of 1984, (SCPA) was enacted, and how will the identified constraints in microlithography effect the near and long-term future of VLSI logic design? Will these constraints impact the expected protection offered by the SCPA?

The report is an industry point of view from Digital Semiconductor, a Business Unit of Digital Equipment Corporation of Maynard, Massachusetts. Digital is a company with 22 years experience in engineering and manufacturing of semiconductor based CPU designs. The last 12 years have been in advanced CMOS semiconductor processes. Digital Semiconductor is a merchant vendor of networking, communication, bridge, graphics and video chips, as well as the Alpha microprocessor.

The assistance of several persons proved invaluable in obtaining a basic understanding of the CMOS process and the manufacturing process and equipments necessary to manufacture state of the art semiconductor chips. I wish to express my gratitude to my immediate supervisor, Evelyn Balch, for her continued support of my education in Intellectual Property at Franklin Pierce Law Center and her contributive comments in reviewing this report.
The writer is responsible for the content and any errors or omissions which may or may not appear.

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Semiconductor Protection Mechanisms: an Industry Point of View

I. Introduction

> Global demand for semiconductors continues to rocket ahead. The orders received during the first quarter were up almost 50 percent compared to the same three months of 1994. Worldwide deliveries are expected to be up 24.6 percent this year, compared to a 31.8 percent jump in 1994.
>
> Henderson Electronic Market Forecast [1]
> April 1995

Digital Equipment Corporation began its semiconductor manufacturing operations in 1974. Its first LSI (Large Scale Integration) facility was opened in 1979 with two 3 inch wafer FABS, one dedicated to Metal Oxide Silicon (MOS) products and the other to Bipolar technology. In 1981 an E-Beam mask shop was completed and the wafer size increased to 4 inch with 3 micron minimum feature size. In 1985 a new FAB 3 was completed to produce 5 inch ZMOS wafers with 1 micron dimensions.

Semiconductor manufacturing plants are built to serve one or two generations of technology and usually have a narrow product base. In 1989 the original FAB 1 was phased out and operations shifted to a new FAB 4, manufacturing 6 inch wafers with .75 micron dimensions. In 1990 FAB 2 was closed. 1994 marked another change with the opening of the newest technology in FAB 6, manufacturing 8 inch wafers with .35 micron dimensions. New technology development is very expensive, the new World-Class FAB 6 took almost three years to build at a cost of more than $500M. To be competitive in such an environment requires very high capital investment. Currently there are 20 world-class FABs around the globe. LSI Logic Corporation is building its major wafer manufacturing facility in Gresham, Oregon. The company's first 8 inch wafer FAB, with 0.35 micron line-widths will be built at a cost of

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about $600M to $800M and it will not be on line until early 1997. The FAB will be designed to produce 14,000 to 16,000 wafers per month. Appendix A details the CMOS manufacturing process.

To make faster computers, the clock speed at which semiconductor chips operate must increase. This means that the transistors must be placed closer together. In order to get the transistors closer together, the entire circuit must be made smaller, now into the submicron area.

This report looks at the Semiconductor Chip Protection Act (SCPA) and the changes that have taken place in semiconductor technology over the last 11 years. The report focuses on the importance of understanding how future changes to the microlithography process, required to further the VLSI miniaturization, will impact the expected protection afforded by the SCPA.

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2. SCPA Overview with a focus on Reverse Engineering

The Semiconductor Chip Act of 1984 was enacted to protect the U.S. semiconductor industry from increased competition, mainly from the Japanese, and to protect the cost of capital investments in their innovative designs. The legislative focus was to protect the "mask work" which contains the physical layout of each layer of electronic circuitry used by the photolithography process in making semiconductor devices.

The following discussion is referenced to the Semiconductor Chip Protection Act of 1984 sections 901 and 906, listed below.

17 U.S.C.A. Section 901 Definitions;

(a) As used in this chapter -

(1) a "semiconductor chip product" is the final or intermediate form of any product -

(A) having two or more layers of metallic, insulating, or semiconductor material, deposited or otherwise placed on, or etched away or otherwise removed from, a piece of semiconductor material in accordance with a predetermined pattern; and

(B) intended to perform electronic circuitry functions;

(2) a "mask work" is a series of related images, however fixed or encoded -

(A) having or representing the predetermined, three-dimensional pattern of metallic, insulating, or semiconductor material present or removed from the layers of a semiconductor chip product; and

(B) in which series the relation of the images to one another is that each image has the pattern of the surface of one form of the semiconductor chip product;

(3) a mask work is "fixed" in a semiconductor chip product when its embodiment in the product is sufficiently permanent or stable to permit the mask work to be perceived or reproduced from the product for a period of more than transitory duration;

Section 906 Limitation on Exclusive Rights: Reverse Engineering; First Sale

(a) Notwithstanding the provisions of section 905, it is not an infringement of the exclusive rights of the owner of the mask work for -

(1) a person to reproduce the mask work solely for the purpose of teaching, analyzing, or evaluating the concepts or techniques embodied in the mask work or the circuitry, logic flow, or organization of components used in the mask work; or

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(b) Notwithstanding the provisions of section 905(2), the owner of a particular semiconductor chip product made by the owner of the mask work, or by any person authorized by the owner of the mask work, may import, distribute, or otherwise dispose of or use, but not reproduce, that particular semiconductor chip product without the authority of the owner of the mask work.

In their article entitled, "*Chip Protection Law May Miss the Mark,*" Michael Ladra and James Otteson [2] ask, "why the SCPA has gone practically unused, especially in the wake of Brooktree's apparently successful application of it." The answer they give is that, "semiconductor designers and manufacturers simply believe the SCPA's protection is inadequate and meaningless." Some in the industry have discontinued filing mask work registration's because they feel they are getting better protection from patents and trade secret protection. This is the position taken by Digital Semiconductor.

Ladra and Otteson point out that since the SCPA allows for reverse engineering a "clone maker" could design a new chip with the "same functionality" as the protected one. They find that the industry use of Computer Aided Design (CAD) and simulation tools make the SCPA "largely irrelevant," they do not have to direct copy anymore.

Similarly, John G. Rauch [3] in his article entitled, "*What's wrong with what Congress gave the Semiconductor Industry?*" also focuses on the "loophole" of reverse engineering and it is his opinion that changes in technology have put the pirates out of business and thus have made the chip act "Moot." This may not be true, although now technically more difficult and expensive, with the high capital investment required for the latest "state-of-the-art" process equipment, reverse engineering is still possible by those having the understanding and skills.

Mr. Rauch reviewed the legislative history of this "loophole" by recounting the difference between piracy and reverse engineering. He defines piracy as the, "photographic reproduction of a first chip and direct incorporation into a second chip," and reverse engineering as, "making improvements to an existing chip by incorporating substantial parts of its design into the second chip."

The problem, as Mr. Rauch points out, is that a "legitimate reverse engineer is given freedom to appropriate the intellectual property of another." He finds that the, "conceptual basis of reverse engineering is inconsistent with other forms of intellectual property. Reverse engineering, as

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originally conceived, was analogous to fair use of a copyrighted work. Fair use is limited to purposes such as criticism, comment, new reporting and teaching. Commercial uses of a copyrighted work, in direct competition with the work itself, are presumptively unfair. Section 906(a)(1) of the ACT reflects a similar understanding of reverse engineering. Only the non-commercial activities of teaching, analysis, and evaluation of a mask work are recognized as legitimate reverse engineering under section 906(a)(1)."

However, Section 906(a)(2) of the Chip Act, adds the commercial exploitation of any results of the reverse engineering effort into the statute. Mr. Rauch finds that this section of the law, the right to distribute, "unique to U.S. intellectual property law." The reverse engineering provision of the Semiconductor Chip Protection Act allows the free appropriation of property clearly protected by the exclusive rights of the statute. Thus, reverse engineering destroys the incentives created by the Chip Act.

Joel Miller [4] offers a warning about some of the "pitfalls of reverse engineering" in his article, "*Reverse Engineering: Fair Game or Foul?*," the scope of protection can be, "not at all obvious, often being a combination of overlapping patents, copyrights, trademarks, and mask-works registrations." He adds, "As a general rule, while it is okay to look, they should be very careful about what they take - and how they take it."

The following quote is from the John G. Rauch [5] article in, IEEE SPECTRUM, titled, "*The Law on Reverse Engineering*,"

> "To stay within the bounds of the chip protection act, the chip copier must prove some innovation was added, and must produce a paper trail"

This "two-legged defense" to infringement, when using reverse engineering, requires that "some degree of innovation" be present in the final design and that a significant paper trail exist to show the development of the ideas as the design progressed.

Mr. Rauch cites the only significant case applying the SCPA, Brooktree v. AMD, a case where the jury ruled AMD's copying of Brooktree's designs were not due to reverse engineering. The paper trail presented did not satisfy the jury either.

Digital Semiconductor uses engineering notebooks to capture initial discoveries and critical key

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dates, however most of the design, simulation and verification is all done on computer systems with backup and archived copies available. The "paper trail" created by one of its new product project teams is substantial and very well documented and protected.

Mr. Rauch suggests that chip manufacturers design their devices to make reverse engineering more difficult with embedded "shapes or patterns" that would only be known to the original owner. In my interviews with design engineers here at Digital Semiconductor, I discovered that given the high cost of real estate, at each layer, non-functioning elements would not be placed within the circuits. Only standard logo's, *M*, or process related identifiers would be allowed, those required by the manufacturing process.. I don't think a "pirate" would copy anything that is not understood. Given the complexity of today's process technology, reverse engineering does not appear to be of any value to anyone, other than learning, unless they understand the manufacturing process and had the FAB to produce the devices.

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3. Changes in Chip Technology Between 1984 and 1995

Today you can have the power of a 1988 vintage Cray Y-MP supercomputer from Cray Research in the form of an Intel Pentium microprocessor.

In the PC of today you get roughly 100 million transistors that pack the wallop of an IBM 3090 mainframe from 1985

Business Week/July 4, 1994

The first Microprocessor was invented by Intel Corp. [6] in 1971. In 1989, they introduced their next generation design of a "superchip" the 80486 (486). This chip held more than 1 million transistors with the performance of an IBM 3090. The Intel 386 chips had circuit lines 2 microns wide (a human hair is 100 microns in diameter). The new 486 chip introduced in 1989 would have a 1 micron line width.

The following chart shows how incremental changes to chip complexity and minimum MOS feature sizes have changed within Digital Semiconductor over the ten year period from 1985 to 1995.

Technology	(microns)	Shipping Date	Transistor count	Die Size(mils)	Pins
ZMOS	3	5/85	125K	353 x 358	68
CMOS-1	2	1/88	180K	384 x 378	84
CMOS-2	1.5	7/89	320K	470 x 470	224
CMOS-3	1.0	10/90	316K	425 x 425	224
CMOS-4	.75	11/91	1,300K	575 x 637	339
CMOS-5	.5	5/95	9,300K	732 x 664	499

Future technology projections

	1993	1996	1999	2002	2005	2008	2011
capacity (megabits/ gigabits)	16	64	256	1024	4	16	64
speed (megahertz)	150	350	400	500	600	700	800
size (micron)	0.5	0.35	0.25	0.18	0.12	0.10	0.08

The future direction of chip technology is spelled out in the article titled, "*Wonder Chips*," a

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special report in Business Week [7]. According to the article, "Getting to the first gigabit generation in 2002 will require only evolutionary improvements in production equipment, but it will take some ground-breaking new technology to go much further." Digital Equipment is one of only a few computer companies that manufacture their own semiconductor devices. As FAB costs continue to rise, fewer state-of-the-art facilities will be built. The strategy for the future is to increase the process yield by getting more "good die" from a single wafer. This is done by moving onto larger wafer sizes, currently 8 inches in diameter, with 212 chips per wafer. The Japanese are already talking about 12 inch wafers.

Since the photomask process is a financially demanding and capital intensive business, many semiconductor manufacturers, like Digital Semiconductor, purchase their masks from photomask speciality houses such as Du Pont Photomask. Mr. John Hodgson [8], Managing Director of DuPont Electronics Materials, of which DuPont Photomask is a business unit, explains why the emerging mask industry is so financially demanding. He points out that, "the latest MEBES 4500 E-beam exposure unit is priced at around $6M, and the Alta 3000 patterning equipment from ETEC Systems is about $5M each. Considering that Du Pont has mask making facilities scattered all over the world, in Europe, the USA, and the Far East, it is necessary to purchase several machines to provide global coverage. Masks will be one of the most critical items in achieving sub-0.25 micron technology in the coming decade, and Du Pont is committed to providing the best technology available."

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4. Protection Mechanisms Available

Digital Semiconductor takes full advantage of all intellectual property protection available to protect its design and manufacturing processes and its product brand names. As a merchant vendor, there are also several legal considerations that must be documented and communicated to the engineering community when dealing with customers and other parties. Non-disclosure agreements (NDA'a) and Product Information Disclosure (PID) Agreements are two protection mechanisms that protect against the loss of patent rights or trade secret information. NDA's protect business and technical information during evaluation of potential business opportunities or pure transfer of information. Standard agreement forms are used without legal involvement when there are no changes to the agreement. If especially sensitive information of either party is going to be disclosed, that may require non-standard terms, then the law department must review the Agreement. Internal and external communication protection mechanisms are in place for business, anti-trust, patent and trade secret reasons to protect sales and keep a competitive edge. Product Information Disclosure Agreements protect the business and intellectual property from premature disclosure of product availability, which Digital could not deliver upon or which could cause a customer to make the wrong purchasing decision, and from the public disclosure of a sale or offer for sale that would start the time allowed (one year) for filing any patent application. Licensing and loan of product agreements are used when more than information, hardware or software source code, etc., is shared for "beta testing" or evaluation purposes by outside organizations.

An intellectual property strategy is in place and is overseen by an Intellectual Property Committee made up of members from different areas of technological expertise including computer architecture, CMOS technology, circuit design, logic simulation, packaging technology, as well as the patent law group. The Committee is chaired by the Technical Director.

PATENTS

Patents are used to guarantee freedom of movement within the semiconductor business and to keep a technical edge over the competition. Patents are also used to leverage cross-licensing of patent portfolios. Patents along with copyright are a good way to promote the engineering

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excellence of Digital Semiconductor. Patents can also be used to influence the setting of industry standards that benefit Digital and the semiconductor industry.

Patents are used to protect the product architecture, circuit designs, packaging of semiconductor chips, manufacturing processes and test software.

COPYRIGHTS

All technical and business literature distributed external to Digital, marketing brochures, schematic drawing, software, etc., such as the Digital Technical Journal.

TRADE SECRETS

This type of protection is the responsibility of the business unit to identify and secure. Processes are in place to properly identify and label all trade secret documents with "Restricted Distribution", "Internal Use Only" or "Confidential."
CMOS Process know-how is kept in the "Tech Files", the process specifications for the manufacture of each specific product. These are known as layout analysis tools, the rule checkers and circuit verifiers are all part of secured databases.
Licensing Agreements and, NDA's are used where process know-how is to remain a trade secret but vendors and third party software developers and hardware vendors are required to know the specifications of our secret processes. Engineering notebooks are used to document and secure engineering discoveries from research. Business information is also secured information. Exit interviews are given to all employees leaving the company to remind them of their commitment to Digital Semiconductor's confidential information.

TRADEMARKS

The protection of all corporate brands, "Brand Identity", falls into the Trademark area of protection. Some categories of trademarks are listed below;

Software, including circuit simulation tools,
Hardware Computer systems "PDP-11",
Modem, "Scholar" and
Services like, Network services,

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Customer Support Services,
Marketing such as Trade Shows like "DECWORLD"
Health Insurance Plan "HMO ELECT"
Architecture "Alpha AXP", design mark
"AlphaGeneration" for Hardware/Software/Services
Buses, "CACHEBUS"
Recruitment Services, "DECexecutive"

Guidelines for the proper use of Digital trademarks are made available to employees on the network.

MASK WORKS (SCPA)

The earliest date of record for a mask work registration within Digital was 6/27/85, for the following products:

Registration number, MW 1274, description, Original layout of an eight-channel asynchronous receiver-transmitter;
Number 1275, description, Original layout of a first chip forming a two-chip CPU;
Number 1276, description, Original layout of a second chip forming a two-chip CPU;
Number 1277, description, Original layout of a memory multiplexer.

Of the hundreds of new designs or the shrinked version of a design, Digital Semiconductor only holds 66 mask registrations in total, with the latest date of registration December 8, 1993, Registration number MW 9-614 for the ALPHA CPU chip. The Law Department put out a memo stating that the mask work registration was no longer required because, "the maskworks filings did not appear to offer any greater protection than Digital was able to obtain through other means."

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5. Future Technology Requirement, Extending Optical Lithography

Does mask work protection rely solely on the photolithography process?

This chapter looks at the physical mask or reticle as we know it today, and a future process that might not use a mask. The Semiconductor Chip Act under section 901, Definitions describe the "mask work" as a series of related images, however fixed or encoded. The statute under 901(A)(3), says that, "a mask work is "fixed" in a semiconductor chip product when it embodiment in the product is sufficiently permanent or stable to permit the mask to be perceived or reproduced from the product for a period of more than transitory duration." If the "fixed or encoded" term means the CAD data stored in a computer, then the future "Xray" or direct write of the pattern will still be protected by the statute. If not then the protection as found in the SCPA would not apply to process that use X-ray writing of the design pattern directly on the wafer.

David Levenson [9], in his article entitled, "*Extending Optical Lithography to the Gigabit Era*" addresses the responsibilities of designers and the industry in understanding what is required to meet the challenges of the sub-half-micron era.

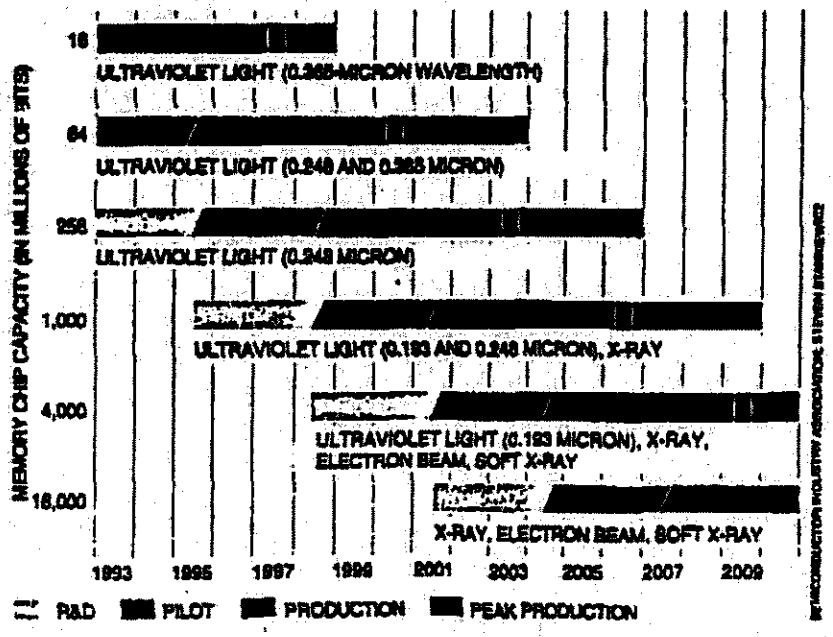


Figure 1. Lithography Development

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Figure 1, shows that by the year 1998, X-rays will be required to meet the requirements of 1/8-micron regime.

Gary Stix [10], in his article entitled, *"Toward "POINT ONE""* raises a concern as to how physicists, chemists and engineers are going to decide how to "advance the technology." The dimensions being worked in the labs today measure .1 and .2 microns, which at .1 micron is one thousandth the width of a human hair. Problems with the photographic process begin to show up at these minute dimensions. Stix suggests that X-rays may be the only way to, "fashioning circuits with billions of transistors." The big question is how to "wring more out of lithography," which is operating at its optical limits.

Other process steps also become more difficult at these dimensions. The build-up of tolerances between several layers of masks leads to alignment problems when dealing in the tens of nanometers. Efforts are under way to develop X-ray systems that will operate at .1 micron or less. However, the use of X-ray, or direct electron beam writing onto the photoresist is done one element at a time instead of the complete die level at one time, this would not be very efficient for a volume manufacturer. The introduction of non-optical lithography would be a major paradigm shift, according to The National Technology Roadmap for Semiconductors [11]. This shift in technology would eliminate the need for any masks. The throughput requirements will still have to be met if this proves the right or only way to advance the technology.

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6. Summary and Conclusions

The SCPA of the 1980's is not seen as a viable protection mechanism in the 1990's by the semiconductor industry because the primary reason given for the creation of the SCPA has basically disappeared. The threat of pirating U.S. chip designs by Japan is not the issue today. The SCPA stopped the direct copying of designs. With the "loophole" of reverse engineering, the SCPA is not accepted as the protection of choice. The significant growth of Computer Aided Design (CAD) tools in the 80's which continued into the 90's, make the design, simulation and testing of complex computer circuits faster, easier, and better protected through internal networked systems with enhanced security mechanisms. With today's technology, even if 100% of the mask was copied, the taker would not benefit unless a complementing process was known and used. The economic bars to entry today, the use of third party vendors supplying some level of process value added, and the sharing of critical information among licensee's, also limits the number of key players. Demand is very high for high-priced microprocessors, microcontrollers and memory chips. The "chip piracy" of the 80's is now called "chip theft" in the 90's. The headlines in the August 13, 1995 Boston Globe read, "Computer chip newest target in white-collar office thefts." The theft of computer memory and microprocessor chips today is not for their intellectual property value but their street value.

Appendix B, received from the Copyright Office, is the ten-year statistics on mask work registrations from 1985 to 1994. The data show that the total number of registrations granted have been declining in the most recent 5 year period, over the period of 1984 to 1990, by some 359 registrations. This fact could be viewed as a lack of confidence in the SCPA. The expectation would be that, due to increases in numbers of new product development, the number of registration would be increasing. For the same period the number of registrations not

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granted, for various reasons, has dropped significantly.

Appendix C, also received from the Copyright Office, is a listing of various companies that filed for mask work registration in 1994. The Japanese are filing for the most registrations followed by a few U.S. semiconductor companies like, Cirrus Logic, Advanced Micro Devices and Texas Instruments. Of interest to this report is the low number of registrations for computer companies such as Digital and IBM at only 2 each and the relatively low number for Intel, one of the largest, if not the largest U.S. computer semiconductor manufacturer.

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Appendix A

Introduction To CMOS Design/Mfg./Verification Process

A brief description of the Complimentary Metal Oxide Silicon (CMOS) manufacturing process. will provide the reader with a better understanding of where the mask work or reticle fits into the total CMOS manufacturing process [12].

The making of an Integrated Circuit.

Here at Digital Semiconductor we purchase our wafers already sliced, polished and coated with what is called its epitaxial layer. The wafers are made from a single silicon crystal ingot grown from high-purity molten silicon, beach sand. Computer aided design (CAD) tools help design the circuitry and interconnections for each layer of the chip. These designs become the pattern of the many photo-masks or reticles, this work which used to be done at the Hudson facility's own "E Beam Generator," is now done by outside vendors.

The manufacturing process, at Hudson, begins with the formation of a thin uniform layer of silicon dioxide using what is called Chemical Vapor Deposition, when Oxygen or water vapor reacts chemically with the silicon wafer surface at high temperatures to form this thin, uniform layers of silicon dioxide. Contacts and interconnects are formed by "sputtering" deposits onto the wafer forming the first of many metal layers.

The first layer using the photolitography process, begins with the application of the photo resist. Figure 2, shows what the wafer surface looks like at this step in the process.

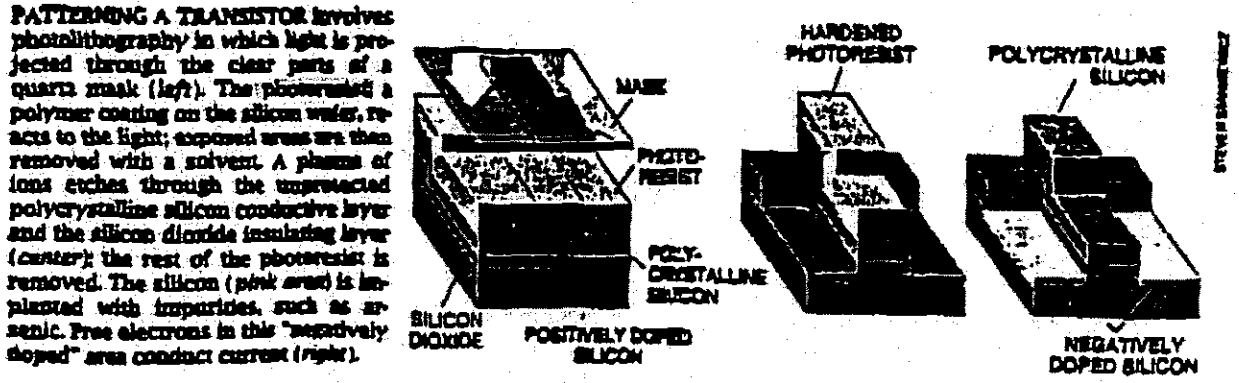
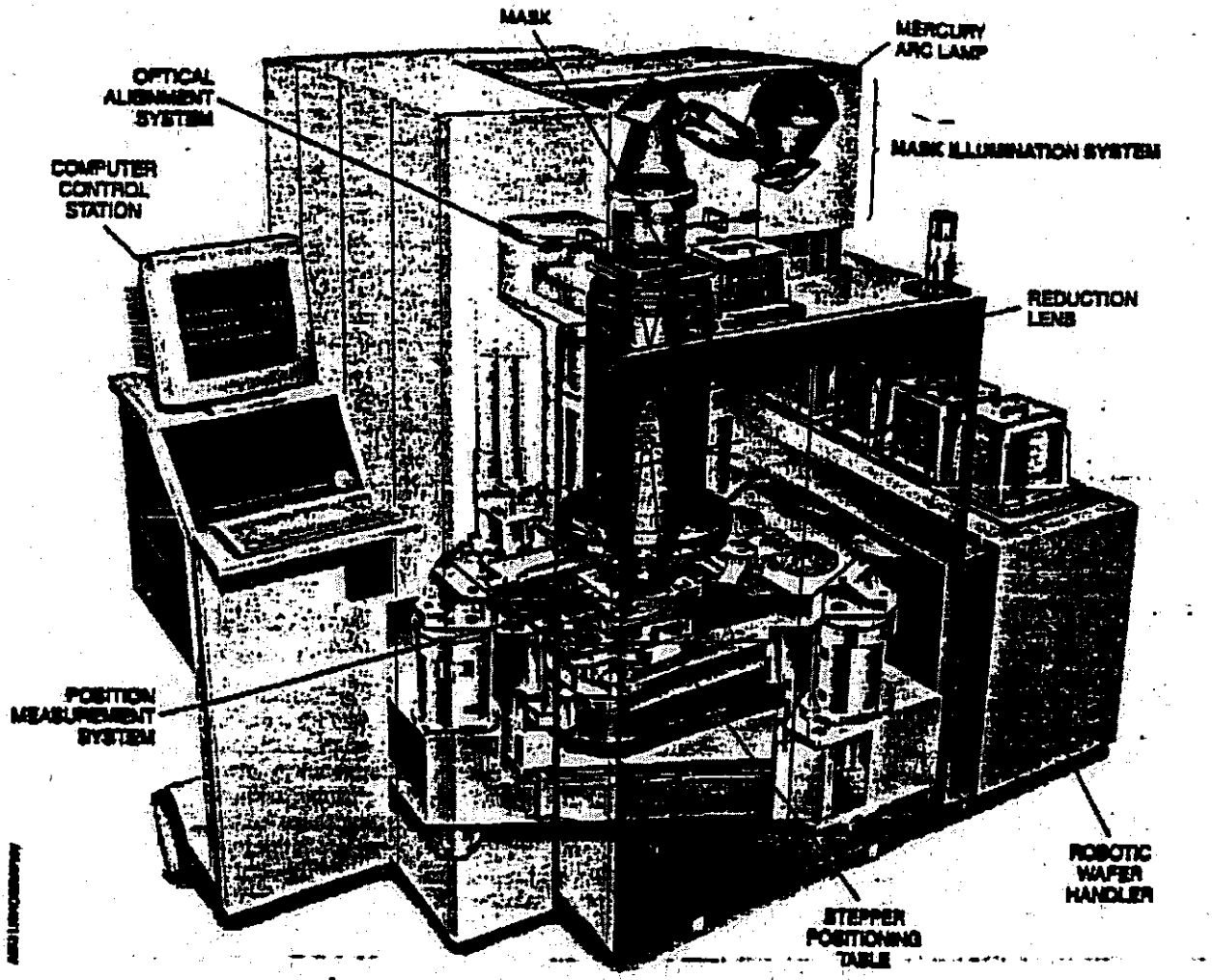


Figure 2. Patterning A Transistor

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Figure 3, is a picture of the pattern stepper, used to expose many patterns across the wafer surface.



STEPPER, or photolithography machine, imprints circuit patterns on silicon wafers. Ultraviolet light from an arc lamp (or from a laser) passes through a mask bearing the image of the circuit. A sophisticated lens apparatus reduces the image and projects it onto part of a wafer. The table then moves, or "steps," to expose other chips.

Figure 3. Stepper

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Once the surface has been "developed" using chemical solutions, baking, and etching away unwanted areas, the process is repeated for another layer.

When the wafer has completed its creation under smoke and fire, it is tested as a wafer using a probing technique which is capable of testing each individual die on the wafer. This is one test to determine the wafer yield, any defect die are so marked. The wafers are then diced into their proper die size using a diamond saw. The die are mounted onto its package surface using a robot arm with a vacuum pickup to gently place the die into the exact center of the package. Robots are again used to accomplish the wire-bonding which connects fine gold wires between the many pads on the chip to pins on the surrounding package. The packages are then sealed and tested.

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Appendix B

TEN-YEAR STATISTICS ON MASK WORK REGISTRATIONS
Page 1, 1985-1994

	5-YR 1985-9	1990	1991	1992	1993	1994	5-YR 1990-4	10-YR Total
Registrations:	5454	1093	1075	988	923	1016	5095	10548
United States	2980	309	478	491	549	457	2284	5264
Japan	2189	759	567	428	325	483	2562	4751
United Kingdom	138	7	8	1	10	5	31	169
Taiwan *	0	0	6	44	22	21	93	93
Canada	59	8	5	5	4	9	31	90
Netherlands	14	1	3	13	10	20	47	61
Germany	18	7	6	5	0	9	27	45
Sweden	22	1	1	0	0	11	13	35
France	16	1	1	0	0	0	2	18
Ireland	9	0	0	0	0	0	0	9
Italy	4	0	0	0	0	0	0	4
Switzerland	1	0	0	1	1	0	2	3
Australia	2	0	0	0	0	0	0	2
Austria	0	0	0	0	1	0	1	1
Belgium	0	0	0	0	1	0	1	1
Finland *	1	0	0	0	0	0	0	1
Korea *	0	0	0	0	0	1	1	1
Not registered:	293	13	29	13	16	13	84	377
United States	228	8	16	7	14	13	58	286
Japan	21	5	8	5	0	0	18	39
Germany	17	0	0	0	2	0	2	19
France	11	0	1	1	0	0	2	13
United Kingdom	7	0	3	0	0	0	3	10
Canada	9	0	0	0	0	0	0	9
Taiwan	0	0	1	0	0	0	1	1
Korea	0	0	0	0	1	0	1	1

Reasons for not registering:

Over two years since first commercial exploitation	122
De minimis	78
Deposit incomplete on 7/1/85 deadline	60
Not a semiconductor chip product	53
Commercially exploited before 7/1/83	33
Claim in circuit board	21
Embodied in another claim	9
Ineligible for protection	2

* Eligibility based on first commercial exploitation in the U.S.

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	1985	1986	1987	1988	1989	5-YR 1985-9
Registrations:	1263	859	1122	1047	1162	5454
United States	717	620	583	530	530	2980
Japan	481	179	491	453	585	2189
United Kingdom	39	20	37	29	13	138
Taiwan *	0	0	0	0	0	0
Canada	5	18	2	14	20	59
Netherlands	10	0	0	3	1	14
Germany	1	0	4	7	6	18
Sweden	6	10	0	2	4	22
France	2	5	3	4	2	16
Ireland	0	4	0	5	0	9
Italy	2	2	0	0	0	4
Switzerland	0	0	0	0	1	1
Australia	0	0	2	0	0	2
Austria	0	0	0	0	0	0
Belgium	0	0	0	0	0	0
Finland *	0	1	0	0	0	1
Korea *	0	0	0	0	0	0
Not registered:	140	26	36	18	73	293
United States	108	9	30	15	66	228
Japan	0	5	6	3	7	21
Germany	17	0	0	0	0	17
France	11	0	0	0	0	11
United Kingdom	0	7	0	0	0	7
Canada	4	5	0	0	0	9
Taiwan	0	0	0	0	0	0
Korea	0	0	0	0	0	0

* Eligibility based on first commercial exploitation in the U.S.

Appendix C

MASK WORK REGISTRATIONS - 1994

Adaptec, Inc.....7

Advanced Micro Devices, Inc.....19

Alliance Semiconductor Corp.....9

Altera Corp.....7

Amtech Corp.....1

Anadigics, Inc.....3

Analog Devices, Inc.....5

Apple Computer, Inc.....15

AuraVision Corp.....1

Brooktree Corp.....4

Cable/Home Communication Corp.....8

Cherry Semiconductor Corp.....15

Chips & Technologies, Inc.....8

Cirrus Logic, Inc.....46

Compaq Computer Corp.....25

Consumer Microcircuits Ltd. (UK).....4

Creative Integrated Systems, Inc.....1

Crystal Semiconductor Corp.....1

Cyrix Corp.....3

David Sarnoff Research Center Inc.....1

DCP Research Corp. (Canada).....1

Delco Electronics Corp.....18

Digital Equipment Corp.....2

Echelon Corp.....2

ESS Technology Inc.....1

MASK WORK REGISTRATIONS - 1994, cont.

Fujitsu Limited (Japan).....52

Fujitsu VLSI Limited (Japan).....27

Gennum Corp. (Canada).....7

Hewlett-Packard.....5

Hitachi, Ltd. (Japan).....39

Holtek Microelectronics Inc. (ROC).....1

Industrial Technology Research Institute.....4

Information Storage Devices, Inc.....3

Integrated Device Technology, Inc.....11

Intel Corp.....4

International Business Machines.....2

Kyushu Fujitsu Electronics Ltd. (Japan).....5

Level One Communications, Inc.....2

Linear Technology Corp.....13

MCNC.....1

Matsushita Electronics Corp. (Japan)...21

Mazda Electronics Corp. (Japan).....1

Micrel, Inc.....5

Micro Linear Corp.....4

Micro Power Systems.....11

Microchip Technology, Inc.....16

Micron Semiconductor, Inc.....3

Mitsubishi Electric Corp. (Japan).....23

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MASK WORK REGISTRATION - 1994, cont.

Sun Microsystems, Inc.....1

TelCom Semiconductor, Inc.....4

Teledyne Components.....3

Telefonaktiebolaget L M Ericsson (Sweden).....11

Texas Instruments, Inc.....24

Texas Instruments Japan Limited (Japan).....25

Toshiba Corp. (Japan).....90

Weitek Corp.....3

Western Design Center, Inc.....6

Westland Aerospace Limited (UK).....1

Winbond Electronics Corp. (ROC).....20

Xilinx, Inc.....38

Yamaha Corp. (Japan).....11

Zilog, Inc.....10

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